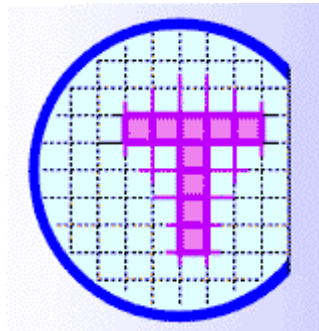


RESEARCH PROFILE



CHiPTec

**The Centre for High Performance Integrated
Technologies and Systems**

**THE UNIVERSITY OF ADELAIDE
AUSTRALIA**

January 2006

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1 The Centre

1.1 About CHiPTec

CHiPTec conducts leading-edge research in high performance microelectronics, mixed analogue and digital circuit design, digital arithmetics and RF systems.

The Centre is one of the longest established microelectronics research centres in Australia, and has a strong record in attracting competitive research grants. In addition to fundamental research, CHiPTec is involved in numerous industry-focussed projects and has forged strong partnerships with organisations both within Australia and overseas.

The core technical capabilities of CHiPTec include:

- High performance VLSI systems
- Mixed analogue and digital circuit design
- Integrated microelectronic RF systems
- Antennas and radio wave propagation
- Digital arithmetic
- Array processor architectures and algorithms

CHiPTec's facilities include state of the art EDA software and workstations for design of microelectronic circuits and a well equipped test laboratory, complete with probing station. The Centre has access to CMOS, SOI and GaAs fabrication, and the Agilent 93000 SOC VLSI test facility.

CHiPTec has been involved in providing education and industry training in microelectronics for more than 20 years. As well as offering technical education, CHiPTec is actively engaged in the promotion of the microelectronics industry and is working to attract and educate engineers to secure the future health of the industry.

1.2 Director's Report

CHiPTec has enjoyed a good year in forging industry collaboration, uncovering new research opportunities, and developing postgraduate education and training.

The Centre has undertaken numerous ARC Linkage and Discovery projects, DSTO research contracts and industry student projects in 2005. The work has significantly strengthened the research partnership with the defence and research development industry, and the microelectronics industry. Major project partners include Ebor Computing, Freescale Semiconductor, DSTO, RADLogic and NHEW R&D.

CHiPTec has embarked upon a major test facility expansion to enhance its chip testing capability. New equipment added include a high-speed data acquisition system and LeCroy waveform analyser. Together with the chip probing station, high performance computing workstations and EDA tools, the facility provide ease of use for normal electronic tests to extreme flexibility for high-speed digital and mixed-signal tests.

Three CHiPTec postgraduates graduated with Ph.D. degree awards and have taken on new challenges. Tae Youn Kim is with Peregrine Semiconductor in Sydney, Lama Chandrasena is with PlanningSA in Adelaide, and Hooman Nikmehr is with Bu Ali Sina University in Tehran.

The Centre continues to attract new postgraduates from Australia and overseas. We welcome five postgraduates. They are Justin Xu from China, Dan Kelly who is our own CSE graduate, Noor Fazila Kamal from Malaysia, Gretel Png from USA and Sunny Yin from China.

I am pleased to report that current postgraduates have been recognised for their quality research on national and international levels. Adriel Cheng has received one of the 2006 Endeavour Australia Cheung Kong Awards that will enable him to visit Tsinghua University for six months. Jonathan Boan has received a Best Student Paper and Presentation award from the Workshop on Applications of Radio Science, Australia, and Bobby Yau was selected to participate in the Young Scientist Program for the International Union of Radio Scientists General Assembly, held in New Delhi.

Cheng-Chew Lim, PhD.
Director, CHiPTec,
January 2006

1.3 The CHiPTec Advisory Board

Professor P.A. Dowd

Executive Dean
Faculty of Engineering, Computer and Mathematical Sciences
The University of Adelaide

Dr. R.J. Clarke

Managing Director
RADLogic Pty Ltd
Australia

Assoc. Professor M.J. Liebelt

Head
School of Electrical and Electronic Engineering
The University of Adelaide

Assoc. Professor C.C. Lim

Director
CHiPTec
The University of Adelaide

Dr. W. Marwood

Research Leader
Defence Science and Technology Organisation
Australia

Dr. J. Yantchev

Managing Director/CEO
Australian Semiconductor Technology Company Pty Ltd
Australia

1.4 Opportunities for Postgraduate Research

Opportunities exist for Masters and Ph.D. level postgraduate projects that fall within the range of the research foci of CHiPTec. Postgraduate degrees are undertaken in collaboration with the School of Electrical and Electronic Engineering at the University of Adelaide.

All initial inquiries should be addressed to: chiptec-admin@eleceng.adelaide.edu.au

Scholarships are available for support of postgraduate students and payment of fees in the University. There is intense competition. Details and application forms for scholarships are available from the University of Adelaide at:

www.adelaide.edu.au/student/postgrad

1.5 Contact

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2 Personnel

Director

Assoc. Professor C.C. Lim

Associate Director

Assoc. Professor M.J. Liebelt

Members

Academic Staff, Research Staff and Industry Partners

Professor D. Abbott

Dr. S.F. Al-Sarawi

Dr. J. Choi
UNSW

Assoc. Professor C.J. Coleman

Mr. S.W. Cumpston
Ebor Computing

Assoc. Professor B.R. Davis

Professor D.A. Gray

Dr. W. Marwood
DSTO

Mr. A.D. Massie
DSTO

Professor J. Mazumdar

Dr. S.P. Mickan

Dr. B.W. Ng

Dr. A.N. Parashkevov
Freescale Semiconductor

Dr. B.J. Phillips

Dr. M.J. Sorell

Mr. M. Trinkle

Professor N. Weste
NHEW R&D P/L

Professor L.B. White

Postgraduate Students

Mr. J. Boan

Mr. N.L. Brine

Mr. A. Burdeniuk

Mr. P. Celinski

Mr. T.K.M. Chee

Mr. A. Cheng

Mr. H.G. Chew

Mr. K.L.C. Chin

Mr. D. Dissanayake

Mr. Y. Gao

Mr. J. Giesbrecht

Mr. A. Hongwitayakorn

Mr. B. Jamali

Ms. N. Kamal

Mr. D. Kelly

Mr. J.H. Kong

Mr. Y. Kong

Mr. Z. Lim

Mr. H. Ma

Mr. G. Malema

Ms. G. Png

Mr. D. Tan

Mr. T. Townsend

Mr. H. Yardley

Mr. X. Yin

Mr. T. Sarros

Mr. K.N. To

Mr. J.X. Xu

Mr. K.S.B. Yau

Mr. Y. Zhu

Visiting Researchers

Professor Joongho Choi
University of Seoul

Professor Manh Anh Do
Nanyang Technological University

Mr. A. Robb
Ebor Computing

Mr. K. Zacher
DSTO

Mr. P. Dabrowski
Ebor Computing

Mr. M. Goss
Ebor Computing

Mr. D. Taylor
DSTO

Associate Members

Dr. S.S. Appleton
Silicon Graphics (USA)

Dr. P. Ashenden
Ashenden Designs

Dr. A.J. Beaumont-Smith
P.A. Semi (USA)

Dr. A.J. Blanksby
Gnome Technologies

Professor N. Burgess
Icera Semiconductor

Dr. L.M. Davis
Macquarie University

Dr. N. Habili
iOmniscient

Professor M. He
Northwestern Polytechnical University

Dr. H. Nikmehr
Bu Ali Sina University

Mr. M. McGeever
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Dr. S.V. Morton
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Dr. A. Omondi
Flinders University

Professor K.L. Teo
Curtin University of Technology

Dr. N. Asgari
Flinders University

Dr. R.J. Beare
CSIRO

Dr. M. Biglari-Abhari
The University of Auckland

Professor A. Bouzerdoum
Wollongong University

Dr. E.W. Chong
Canon CSIRA

Professor. K. Eshraghian
Planar Photonics

Dr. G.P. Harmer
Sensor Research & Development (USA)

Dr. C.J. Howland

Dr. W.K. Lin
Silicon Integrated Systems (Taiwan)

Dr. A.R. Moini
Silverbrook Research

Dr. X.T. Nguyen
DSTO

Dr. R. Sarmiento
Universidad de Las Palmas

Professor W. Zhao
Texas A.&M. University

3 Research Activities

Research activities of the Centre may be grouped into the areas listed below.

Research in Microelectronic Systems

- Digital Microelectronic Systems
- Mixed Analogue-Digital VLSI
- Information Security
- Digital Arithmetic
- Design Verifications and Tests

Research in RF and Wireless Systems

- Wireless Networks
- Antennas and Radio Wave Propagation

Research in Imaging

- Insect Vision
- Photonics
- Wavelet Techniques and Applications

Within each category, a list of current projects is given. While the project descriptions give some detail of the Centre's activities, it is worth emphasising that the individual-based research often forms part of major team-oriented projects designed to encourage collaborative and inter-disciplinary work.

3.1 Digital Microelectronic Systems

3.1.1 Multi-Channel Reconfigurable High Dynamic Range Digital Receivers

(Contact: Dr. C.C. Lim, cclim@eleceng.adelaide.edu.au)

Wireless systems will increasingly require much higher levels of performance, in the form of abilities to receive and to distinguish signals from multiple sources that are physically close together and transmit on similar frequencies. In this project we develop a test system that will allow us to undertake research on new algorithms that will achieve these higher levels of performance. Our objective is to demonstrate dramatic improvements in the capacities of receivers for defence surveillance and future generation mobile phone systems. We have designed for CMOS fabrication a high-precision digital down converter (DDC) chip with internal bus widths and arithmetic to allow the exploitation of spatial dynamic range enhancement. Under development is a multi-channel reconfigurable high dynamic range digital receiver to be used in a remote and distributed environment. An immediate application is for improved multi-channel processing in LLISP ionosonde. The test system will be configured to analyse wideband vector signals for devising signal detection and separation algorithms in OFDM systems.

Support: Australian Research Council, Ebor Computing, Defence Science and Technology Organisation

3.1.2 High Speed Processor Architectures for Machine Learning Algorithms

(Contact: Dr. C.C. Lim, cclim@eleceng.adelaide.edu.au)

Support vector machine (SVM) is a learning algorithm. Its major use has been for supervised classification. In order to obtain good generalisation in practical applications, an enormous number of examples for training are required. This places huge computational demand on conventional hardware. Since the formulation of SVM is inherently a dense matrix quadratic optimisation problem, we can extend our earlier work on high performance parallel matrix processors to devise parallel processing architectures and algorithms for running machine learning algorithms at computing rates that are orders of magnitude faster than is currently feasible. These architectures and algorithms are applicable to problems such as automatic channel classification in wideband communications systems, and feature recognition in radar images.

Support: Australian Research Council, Lucent Technologies, The University of Adelaide

3.1.3 Pattern-Based Accelerators For High-Speed Signal Processors

(Contact: Dr. C.C. Lim, cclim@eleceng.adelaide.edu.au)

Real-time signal processing applications all have two things in common. They perform repetitive tasks on incoming data, and they require low overhead computation. To reduce memory access overhead it is already common for signal processing systems to have pattern-based address sequencers. This research applies this concept to other tasks to further reduce overhead and improve performance in a multiprocessor developed for multi-channel software radio algorithms.

Support: APA, The University of Adelaide

3.2 Mixed Analogue-Digital VLSI

3.2.1 Mixed Analogue-Digital Design

(Contact: Dr. S.F. Al-Sarawi, alsarawi@eleceng.adelaide.edu.au)

Mixed signal behavioural modelling is becoming more important as the complexity of the analogue portions of VLSI systems increases. In this project design and modelling of mixed analogue-digital VLSI systems are investigated. The design methodologies for complex mixed signal systems are analysed and issues such as digital noise are addressed. The design and modelling procedures are being applied to imager and data acquisition system designs. These systems contain complex analogue and digital functional blocks that require design reliability improvement and reduction in design time.

Support: The University of Adelaide

3.2.2 Wireless Microvalve for Biomedical Applications

(Contact: Dr. S.F. Al-Sarawi, alsarawi@eleceng.adelaide.edu.au)

This program will investigate and perform an in-laboratory proof-of-concept demonstration of a polymer microvalve that can operate by a remote control radio signal. This will be a wireless microvalve that does not require a battery power source. This advance in the technology and scientific knowledge will have important applications for humankind ranging from drug delivery services through to valves in chips that can perform microfluidic chemical analysis. A far reaching long-range vision is its use in electronically

reversible male fertility control. The community benefit in terms of novel biomedical devices and the resulting large international commercial market is significant.

Support: Australian Research Council

3.2.3 A Low Power Transmitter for Remote Monitoring Applications

(Contact: Dr. S.F. Al-Sarawi, alsawari@eleceng.adelaide.edu.au)

The field of wireless communications has been experiencing tremendous growth recently as the numerous advantages have made many applications wireless. Due to the limited power available, wireless products have to consume very little power. This requirement presents designers with a very challenging task considering the Gigahertz frequencies at which those products are meant to function. This research looks into the feasibility of designing a very low power transmitter in CMOS and SOI technologies for remote monitoring applications such as temperature sensing. The transmitter will operate in the 2.4GHz ISM band. Furthermore, to improve the system immunity to noise and interference a Spread spectrum transmission is used. The output power level of interest ranges between 10mW to 100 mW rms for reliable transmission. Consequently, very efficient power amplifiers and back-end circuitry such as ADCs are needed due to the power constraints.

Support: The University of Adelaide

3.2.4 Mixed Analogue-Digital Circuits in Radio Frequency Identification

(Contact: Dr. S.F. Al-Sarawi, alsarawi@eleceng.adelaide.edu.au)

The research investigates new design techniques for low power and low voltage mixed mode analogue-digital circuits using CMOS VLSI technology for a commercial radio frequency object identification system. The integration of all circuitry on a single substrate has a lot of benefits such as improving the system reliability, reducing the system size, increasing inter-system communication speed and making system implementation more cost effective. On the other hand, some difficulties arise as most CMOS technologies are tuned towards digital circuit design and have a wide spread in transistor parameters. The research is concentrating on techniques for designing low power, low voltage analogue and digital circuits for implementation in standard CMOS technologies.

Support: The University of Adelaide

3.3 Information Security

3.3.1 Residue Number System Hardware for Public-Key Cryptography and E-Security

(Contact: Dr. B.J. Phillips, phillips@eleceng.adelaide.edu.au)

Public-key cryptography (PKC) is an important element of electronic information security (e-security). However, the computational complexity of public-key operations can limit the quality of service of security systems based on this technology.

This project will produce new arithmetic algorithms and hardware architectures to perform PKC. An arithmetic structure called the Residue Number System (RNS) will be used to improve PKC implementation on devices such as smart cards and e-commerce servers. The new designs will offer improvements in speed and security.

Support: Australian Research Council

3.4 Digital Arithmetics

3.4.1 Fast Parallel Multiplier Design

(Contact: Mr. M.J. Liebelt, mike@eleceng.adelaide.edu.au)

The development of the single-chip multiplier has been one of the key innovations spurring the massive recent growth of graphics and DSP hardware. These chips (and CPUs to a lesser extent) benefit greatly from any improvement in speed or throughput/area that can be made to the multiplier design. Tree-based multiplier schemes are the fastest known, but significant difficulties occur in determining the optimal tree structure for a given problem. Our work looks to overcome these on two fronts – by improving the speed of an optimal tree-finding heuristic and by finding better algorithms for generating near-optimal reduction trees. There is also an opportunity for work designing matched final adder structures.

Support: The University of Adelaide

3.4.2 Architectures for Floating-Point Division

(Contact: Dr. C.C. Lim, cclim@eleceng.adelaide.edu.au)

This research investigates a novel architecture for floating-point dividers targeting for CMOS VLSI technology. Refinement in the traditional SRT algorithm, a type of non-restoring digit recurrence division algorithm, and the development of optimised architecture for radix-4, radix-16 and radix-10 (decimal) are investigated. A new on-the-fly summation algorithm has been developed and realised.

Support: The University of Adelaide, Government of Iran

3.4.3 The Design of Arithmetic Systems using the Residue Number System

(Contact: Dr. B.J. Phillips, phillips@eleceng.adelaide.edu.au)

The residue number system (RNS) has long been known as an efficient means of implementing multiplication, addition and subtraction; however, other basic arithmetic operations such as division, magnitude comparison and scaling are usually seen as too inefficient in RNS to make the system attractive for all but a very few specialized applications. Recent advances in RNS theory are beginning to change this view and RNS implementations of digital signal processing and cryptography are beginning to emerge. This project aims to advance the theory of RNS through investigation of the underlying arithmetic and also through implementation of systems employing RNS.

3.4.4 Arithmetic Data Value Speculation

(Contact: Dr. B.J. Phillips, phillips@eleceng.adelaide.edu.au)

Modern computers frequently use guesswork. Rather than wait for an exact result they guess the outcome and race ahead, speculatively executing code. Guesswork of this kind is widely used to predict true or false conditions and data loaded from memory, but is not yet applied to results of arithmetic operations. However the quest for even faster computers is set to see data value speculation become an important technique.

The design of small, fast arithmetic units to produce estimated results is a new and exciting avenue of research. This project will see a variety of these units built and tested. It will also explore new microprocessor architectures to take advantage of arithmetic speculation.

Support: The University of Adelaide

3.4.5 Design of High Performance, Compact, Low Power Arithmetic Systems Based on Threshold Logic

(Contact: Prof. D. Abbott, dabbott@eleceng.adelaide.edu.au)

In recent years, there has been renewed interest in threshold logic, mainly as a result of the development of a number of successful implementations of CMOS threshold logic gates. Threshold logic enables the design of digital integrated circuits with a significant reduction in transistor count, area and power dissipation, and improved speed performance. In this project, we investigate the design of arithmetic circuits including parallel counters, adders and multipliers based in two high performance threshold logic gate implementations which we have developed.

Support: The University of Adelaide

3.5 Design Verifications and Tests

3.5.1 Hardware Verification Techniques for Complex High Performance Systems-on-chip

(Contact: Dr. C.C. Lim, cclim@eleceng.adelaide.edu.au)

Verifying the correctness of modern integrated circuit designs is a critical success factor from both economic and technological perspectives. Rapid advances in semiconductor manufacturing technology are not matched by similar gains in hardware design verification methodology. This creates a widening verification gap that threatens the viability of future complex ICs. This project aims to address this issue by developing novel hardware verification techniques targeting complex high performance systems-on-a-chip. The research outcome will be a set of verification techniques and tools that directly benefit the advancement of future IC development, verification and manufacturing. The research is built on the verification flow SALVEM (software application level verification methodology). Conceptually, SALVEM uses embedded software applications to excite interactions across multiple software and hardware layers of the SoC architecture. Test generation and coverage are two main functions performed by SALVEM. Our application test cases are generated using small modular segments of common software SoC code, called snippets. Coverage makes use of control graphs and symbolic trajectory evaluation techniques.

Support: Australian Research Council, Freescale Semiconductor Australia, Australian Postgraduate Awards

3.5.2 Testability Properties of Asynchronous Circuits

(Contact: Mr. M.J. Liebelt, mike@eleceng.adelaide.edu.au)

Asynchronous digital circuits have several potential advantages over synchronous circuits and there is a great deal of current research on asynchronous design methods. If asynchronous methods are to be widely accepted it is necessary that comprehensive CAD tools be developed and that there be efficient test techniques for VLSI asynchronous

circuits. There has been and is a lot of research on test methods and design for testability of synchronous circuits. Some of these techniques are applicable to asynchronous circuits, particularly to data path sections, but with most modern asynchronous design methods the control circuits have very different characteristics to synchronous control circuits. Novel approaches to testing asynchronous control circuits are often required. Fortunately, many asynchronous control circuits possess properties that make them somewhat self-checking. The existing body of results, however, is limited in scope, addressing only stuck-at faults and a useful, but limited range of synchronous circuits. In this project we are seeking to extend the scope of the existing self-checking results, to develop results for fault models which are more realistic than the stuck-at fault model and to establish design for testability guidelines and test strategies for VLSI asynchronous circuits.

Support: The University of Adelaide

3.6 Wireless Networks

3.6.1 Efficient Digital Receiver Design

(Contact: Dr. S.F. Al-Sarawi, alsarawi@eleceng.adelaide.edu.au)

The research investigates efficient digital receiver designs for direct and low intermediate frequency conversion. This would result in bringing the digital signal processing closer to the RF front end and hence an efficient utilisation of the high-density integration of digital design. Variable centre frequency bandpass sigma-delta modulator implementation in silicon-on-insulation and silicon-on-sapphire processes are under investigation. The performance factors under investigation are high-speed conversion at low power and small area.

Support: The University of Adelaide, St. Jude Medical (USA)

3.6.2 Downlink Transmission for Orthogonal Frequency and Code Division Multiplexing Systems

(Contact: Dr. C.C. Lim, cclim@eleceng.adelaide.edu.au)

With the rapid progress in telecommunications, more and more services are provided on the basis of broadband communications, including mobile communications. In order to satisfy the high data rate requirement and efficiently support multimedia services, the modulation and multiple access scheme must be much more spectrally efficient than the current mobile systems. This research aims to develop the combination of adaptive techniques, such as the adaptive modulation and coding scheme and adaptive frequency allocation scheme, with optimal power control so that the spectral efficiency of the mobile system would be substantially increased.

Support: The University of Adelaide

3.6.3 Distributed Sensor Networks

(Contact: Dr. B.W. Ng, bwng@eleceng.adelaide.edu.au)

A wireless sensor network is a collection of a large number of densely scattered sensor nodes which can be networked and deployed in various applications, from tracking and surveillance to environmental monitoring and equipment maintenance. This project involves coordinating networks of inexpensive sensors for information collection and processing. The specific application is in the design and implementation of a collaborative

signal processing framework for multi-target tracking.

Support: The University of Adelaide

3.6.4 Self-Organising Wireless Mesh Networks With Variable Connectivity

(Contact: Dr. C.C. Lim, cclim@eleceng.adelaide.edu.au)

We address wireless networks which are self-organising, self-configuring and distributed to avoid a central point of failure. The nodes in the network carry traffic of different types, and have different connection characteristics and mobility patterns. We investigate self-organising approaches to node clustering for robust interconnection, multipath routing for better reliability, and cross-layer radio resource management using only limited information for optimal wireless utility and better network service. The research outcomes are advanced wireless mesh networking methodologies applicable to the home environment to support elderly and disabled care, office environment to improve productivity and public environment for surveillance.

Support: The University of Adelaide

3.6.5 Millimetre Wave Communication Systems for Consumer Applications

(Contact: Professor D. Abbott, dabbott@eleceng.adelaide.edu.au)

The key outcome of this cross-disciplinary project will be a prototype single-chip (RF section), short-range, 1Gigabit/second, wireless network operating at 60 GHz. This will employ new Silicon Germanium technology in a “system on chip” methodology that will pave the way for low-cost consumer applications of such technology. A new design flow will be developed to support this project, which will enable first silicon pass correct design of complete mm-wave millimetre wave radios on a single chip, a feat that has yet to be demonstrated. A new communication system will be developed to support the high data rates proposed. The significance will be application in very high speed high-bandwidth wireless local networks.

Support: Australian Research Council, NHEW R&D Pty Ltd, Peregrine Semiconductor Australia Pty Ltd, Cadence Design Systems

3.7 Antennas and Radio Wave Propagation

3.7.1 Compact Antennas

(Contact: Dr. C.J. Coleman, ccoleman@eleceng.adelaide.edu.au)

An increasing number of RF systems require antennas that can be incorporated with the electronics into a small package. This can necessitate novel approaches, including the use of active antenna elements. Furthermore, because the antenna environment is often unpredictable, the antennas will need to work well under a variety of conditions. This project seeks to develop compact antennas for a variety of applications and also techniques that can be used to analyse their performance within complex environments.

Support: The University of Adelaide

3.7.2 The Effect of Ionospheric Irregularity upon Radar and Communications Systems

(Contact: Dr. C.J. Coleman, ccoleman@eleceng.adelaide.edu.au)

This project aims to develop the theoretical connection between anomalies in radio wave propagation and disturbances in the ionosphere that supports this propagation. Such anomalies can cause deterioration in the capabilities of communications and radar systems and the aim of the project is to develop irregularity mitigation strategies.

Support: Defence Science and Technology Organisation

3.7.3 Propagation Techniques for Mobile Communication

(Contact: Dr. C.J. Coleman, ccoleman@eleceng.adelaide.edu.au)

This project seeks to develop propagation techniques based on the reciprocity principle. Such techniques have the potential to greatly accelerate propagation calculations and hence allow complex environments to be assessed. The practical application is mainly directed towards the analysis of mobile communication in the urban environments.

Support: Defence Science and Technology Organisation

3.8 Insect Vision

3.8.1 Artificial Insect Vision Chips

(Contact: Prof. D. Abbott, dabbott@eleceng.adelaide.edu.au)

The objective is to map insect vision algorithms onto VLSI to make smart collision avoidance chips. Our goal is to apply the latest neurophysiological models using contrast adaptation.

Support: Australian Research Council, Sir Ross & Sir Keith Smith Foundation, AFSOR (USA)

3.8.2 Millimetre-wave Insect Vision

(Contact: Prof. D. Abbott, dabbott@eleceng.adelaide.edu.au)

This project is researching a novel motion detector utilising a millimetre-wave array front-end with signal processing that mimics insect vision. The use of passive millimetre-wave detection enables a significant improvement over optical or infrared wavelengths when rain, steam or other aerosols obscure a colliding object. This, for instance, used as a blind-spot detector, will enhance driver safety in poor weather conditions. As insect vision techniques do not attempt to process an image, but rely on tracking moving edges, the processing tasks are less hardware intensive resulting in a compact low-cost solution. We are also investigating the use of stochastic resonance to improve the detected signal to noise ratio.

Support: Australian Research Council, Sir Ross & Sir Keith Smith Foundation

3.9 Photonics

3.9.1 TeraHertz Cell Cluster Imaging

(Contact: Dr. S.P. Mickan, spmickan@eleceng.adelaide.edu.au)

With this program, Australia will benefit from the interaction between physics, engineering, biology and medicine to develop a new TeraHertz imaging system. The project will identify the factors that contribute to TeraHertz contrast in soft tissue cell cultures, thereby developing a non-invasive imaging system to show contrast between diseased and healthy cells. This is a fundamental step towards a system for diagnosing disease states of skin cells, for example, the early detection of melanoma. Ultimately, Australia will benefit from a new technology, and new diagnostic biomedical techniques, for rapid, non-invasive and reliable skin cancer diagnosis.

Support: Australian Research Council

3.9.2 Ultra High Speed Photonic Data Converters

(Contact: Dr. S.F. Al-Sarawi, alsarawi@eleceng.adelaide.edu.au)

This project involves novel designs for very high-speed data converters using Self Electro-optic Effect Device. The project has two main streams, the first is the design of novel architectures for Nyquist rate analog-to-digital converters that operate at 10-50 GSamples per second with four to five bits of resolution, while the second stream is concerned with novel data converters that operate at a similar number of samples per second with much higher resolution in the order of 16-20 bits. The latter is achieved by trading the resolution in time for the required bit resolution, hence over sampling data converter principles are utilised. The project involves designs at a number of system design levels that include architectural, circuits and device level. The application of the over sampling converters are in wideband communications surveillance systems and digital radio receivers, which require high speed, high resolution and high linearity data converters. The high speed Nyquist rate data converter are used in generic wideband electronic systems that require very high speed converters but with less demanding specifications for resolution and linearity.

Support: Defence Science and Technology Organisation

3.9.3 Modelling and Measurements of Biomolecules in the T-ray Band

(Contact: Dr. S.P. Mickan, spmickan@eleceng.adelaide.edu.au)

Making measurements on biomolecules, such as proteins, using T-ray radiation is limited by dense spectra and high power loss. This project aims to increase the sensitivity of T-ray measurements so proteins held in organic solvent suspension can be characterised using T-rays, thus revealing resonances that correspond to their 3D structure.

Support: Australian Research Council

3.10 Wavelet Techniques and Applications

3.10.1 Wavelet-based Texture Segmentation

(Contact: Dr. B.W. Ng, bwng@eleceng.adelaide.edu.au)

Textures are an important cue in image understanding. Segmentations of regions based on textural information have been a long-standing problem in computer vision. In this project, the aim is to find robust, reliable segmentation algorithms with wavelet-based techniques. Wavelets have evolved from classical Fourier techniques and have developed rapidly in the last decade to become a versatile, useful tool for joint time-frequency analysis. They have been successfully employed in a range of image processing problems with good success and they possess a number of desirable mathematical properties suitable for image texture analysis. Much of the emphasis of the current project is placed on the texture features that can be extracted from wavelet transforms. One of our main goals is to have a computationally efficient method to perform texture segmentations. We have devised an algorithm that produces high quality segmentations in our experiments. Applications for texture segmentation include surveillance and medical image analysis.

4 Grants and Contracts

Research grants and research contracts operational in 2005 are as follows.

Period	Title	Granting Body	Amount
2002-2005	Multi-channel reconfigurable high dynamic range digital receivers (Lim and Liebelt)	ARC Linkage Ebor Computing DSTO	\$390k
2003-2007	3-D radar propagation model (Coleman)	DSTO Research Contract	\$165k
2004-2007	Hardware verification techniques for systems-on-chip (Lim and Liebelt)	ARC Linkage Freescale Semiconductor	\$180k
2005	Arithmetic unit design for data value speculation (Phillips)	ECMS Small Research Grant Scheme	\$5.5k
2005-2007	Wireless micro valve for biomedical applications (Al-Sarawi)	ARC Discovery	\$198k
2005-2007	Residue number system hardware for public-key cryptography and E-security (Phillips)	ARC Discovery	\$160k
2005-2009	Tera Hertz cell cluster imaging (Mickan and Abbott)	ARC Discovery	\$800k
2005-2007	Millimetre wave communication systems (Abbott and Westle)	ARC Linkage NHEW R&D. ARC grant held at Maquarie University	\$1.65M

5 Collaboration

5.1 Industry Partners

Listed below are major industry partners in 2005.

Industry Partner	Activity
Ebor Computing	ARC Linkage Multichannel Receivers project
Freescale Semiconductor	ARC Linkage SoC Hardware Verification project
DSTO	ARC Linkage Multichannel Receivers project
DSTO	Research contract Radar Propagation Model project
RADLogic	Clock Tree Insertion project
NHEW R&D	ARC Linkage Millimetre Wave project
Cadence	EDA tools for chip design, simulation and analysis
Synopsys	EDA tools for chip design, simulation and analysis
NNTTF	Tele test facility for SoC and high speed chips
MOSIS	Chip fabrication

5.2 Visitors

International visitors were Professor Joongho Choi of University of Seoul on a one-year visit and Professor Manh Anh Do of Nanyang Technological University on a two-month visit. On short term visits were Professor Paul Franzon of North Carolina State University, Professor He Mingyi of Northwestern Polytechnical University, Professor Vojin G. Oklobdžija of University of California Davis, Professor Wu Zhang of Shanghai University, Dr Graham Jullien of University of Calgary and Mr Darence Tan of Synopsys Singapore.

Interstate visitors include Dr Chris Nicol of Agere Systems Australia, Professor Adam Osseiran of Edith Cowan University, Professor Iven Mareels and Dr Jingxin Zhang of Melbourne University, and Professor Jack Singh of Victoria University.

6 Biographies

Cheng-Chew Lim, Ph.D. (Lough.), B.Sc.(Eng) (Hons) (Lough.), S.M.I.E.E.E.
Director, CHiPTec
Deputy Head, School of Electrical and Electronic Engineering, the University of Adelaide
Associate Professor, the University of Adelaide
Associate Dean International, Faculty of Engineering, Computer and Mathematical Sciences, The University of Adelaide
Member, Board of Management, National Networked Tele Test Facility

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Associate Director, CHiPTec
Head, School of Electrical and Electronic Engineering, the University of Adelaide
Associate Professor, the University of Adelaide
Director, Spire Innovations Pty Ltd
Director, Aitec Pty Ltd
Director, Electronics Industry Association
Member, Technical Advisory Committee, National Networked Tele Test Facility

Derek Abbott, Ph.D. (Adel.), B.Sc.(Hons) (Lough.), F.I.E.E.E.
Director, Centre of Biomedical Engineering, the University of Adelaide
Professor, the University of Adelaide

Said Al-Sarawi, Ph.D. (Adel.), B.E. (Alex.), M.I.E.E.E.
Lecturer, the University of Adelaide

Jinho Choi, Ph.D. (K.A.I.S.T.), M.S.E. (K.A.I.S.T.), B.E. (Sogang), S.M.I.E.E.E.
Senior Lecturer, University of New South Wales

Christopher Coleman, Ph.D. (Lond.), B.Sc. (Lond.), D.I.C. (Lond.), B.E. (Adel.)
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Stuart William Cumpston, B.Sc.(Hons) (Adel.)
Managing Director, Ebor Computing

Bruce Davis, Ph.D. (Adel.), B.E.(Hons) (Adel.), B.Sc. (Adel.)
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Douglas Gray, Ph.D. (Adel.), B.E.(Hons) (Adel.), B.Sc. (Adel.)
Professor, Electrical and Electronic Engineering, the University of Adelaide
Deputy Director, CSSIP

Warren Marwood, Ph.D. (Adel.), B.E.(Hons) (Adel.), B.Sc. (Adel.)
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Angus Massie, M.Sc. (George Mason), B.E. (Adel.), B.Sc. (Adel.)
Professional Officer, Defence Science and Technology Organisation

Sam Mickan, Ph.D. (Adel.), B.E.(Hons) (Adel.), B.A. (Adel.)
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Brian Wai-Him Ng, Ph.D. (Adel.), B.E.(Hons) (Adel.), B.Sc. (Adel.), M.I.E.E.E.
Lecturer, the University of Adelaide

Atanas Parashkevov, Ph.D. (Adel.), M.E.E. (Technical University Varna)
Principal Staff Engineer, Freescale Semiconductor

Braden Phillips, Ph.D. (Adel.), B.E.(Hons) (Adel.), B.Sc. (Adel.), M.I.E.E.E.
Lecturer, the University of Adelaide

Neil Weste, Ph.D. (Adel.), B.E.(Hons) (Adel.), B.Sc. (Adel.), F.I.E.E.E.
Director, NHEW R&D P/L

Langford White, Ph.D. (Q'ld.), B.E. (Q'ld.), B.Sc.(Maths) (Q'ld.)
Professor, Communication Networks, National ICT Fellow, the University of Adelaide

7 Publications

Book Chapters 2005

Chew, H.G., Lim, C.C. and Bogner, R.E. "An implementation of training nu-support vector machines", Chapter 7 in *Optimization and Control with Applications*, Qi, Teo and Yang (eds), Springer, NJ, 2005, ISBN: 0-387-24254-6, pp. 157-181.

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Cheng, A., Parashkevov, A., and Lim, C.C.: A software test program generator for verifying system-on-chips, *10th IEEE International High Level Design Validation and Test Workshop 2005 (HLDVT05)*. Napa Valley, California: IEEE Computer, 2005, pp. 79-86.

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Patents 2005

Electrically controlled very high value floating CMOS resistor

Inventor: Said Al-Sarawi

Appl. No.: 10/487,795

Patent No.: US 6,897,528 B2

Date of Patent: May 24, 2005.

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CHU, Eric, Master of Engineering Science,
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BIGLARI-ABHARI, Morteza, Doctor of Philosophy,
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CHONG, Eric Wai-Shing, Doctor of Philosophy,
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MatRISC: a RISC Multiprocessor for Matrix Applications (2002)

HABILI, Nariman, Doctor of Philosophy,
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ASGARI, Nasser, Doctor of Philosophy
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SANTOSO, Agus, Master of Engineering Science
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KIM, Tae Youn, Doctor of Philosophy
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